ANAN-8000DLE

The ANAN-8000DLE HF & 6M 200W SDR Transceiver meets and exceeds the requirements of even the most discerning Amateur Radio Operator, it is based on the work of the OpenHPSDR community.

Keeping in mind the various requirements posed by new cutting edge technologies implemented in the radio it has been designed from scratch, the design successes of the previous generation hardware has been improved in the new implementation.

The ANAN-8000DLE uses an entirely new redesigned transmit chain keeping in mind PureSignal (Predistortion), the result is astounding IMD performance, the typical transmit IMD distortion is about a 1000 times lower than that achieved by a typical modern transceiver available today. It is the world's first Amateur Radio transceiver to use a 50v LDMOS device in the finals.

The ANAN-8000DLE includes two phase synchronous front ends to enable Diversity reception,

An internal four phase low noise boost supply is used to convert 13.8v to 50v for the finals, this enables the user to have the flexibility of using industry standard 13.8v DC as well as battery power whilst at the same time the radio provides all the advantages of the 50v LDMOS amplifier.

The front panel Display is microprocessor driven and displays all critical parameters such as Forward and Reflected Power, SWR, Current, Voltage, Temperature. The microprocessor also provides real time protection for all these parameters.

General Specifications:

- Architecture: Direct Sampling DDC/DUC Transceiver
- Interface: Ethernet
- Phase Noise (Clock): -149dB @ 10Khz
- TCXO Stability (Typical): +/- .1 PPM
- Modes: CW, SSB, NFM, AM, Digital
- Antenna Ports: Three SO-239 50 ohms Software Configurable Ports, One BNC for RX2
- Frequency Resolution: 1 Hz

Electrical Specifications:

- 13.8v DC @ 35A, 3A Receive/35A Transmit

Mechanical Specifications:

- 12Kg (approx. Weight)
- Dimensions: 483MM (L) x 123MM (H) x 320MM (D) (Not including extrusions)
- Stainless Steel Chassis and Aluminum Heatsink

Receiver Specifications:

- Receiver Architecture: Direct Down Conversion
- Dual 16 bit Phase Synchronous ADCs
- Independent filter banks for each ADC
- 10/6M LNAs
- Frequency Coverage: 9Khz to 60Mhz
- Attenuator: 1-30dB step attenuator
- Reciprocal Mixing Dynamic Range (RMDR): 116dB @ 2Khz
- Receiver Phase noise: -149dB @ 10Khz
- Image rejection: 100dB
- Hardware support for 7 independent receivers assignable to either ADC

Transmitter Specifications:

- Transmitter Architecture: Direct Up Conversion
- DAC Resolution: 16 bit
- RF Output Power: 1-200W SSB, CW, FM, RTTY, Digital; 1-50W AM
- IMD: IMD3 typically -72dB @ 200W output on 20M
- Harmonics: Typically better than -50dBc on HF and -60dBc on 6M
- Carrier and Opposite Sideband Suppression: Better than -80dBc
- Transverter IF Output: 0db to +15dB

IOs:

- RCA Line In, Line Out, PTT in, PTT Out
- DB9 Seven Software configurable Open Collector Outputs
- BNC XVTR TX Out, 10Mhz Reference Input
- 6.25mm Barrel Mic, CW Key, Headphones and Speaker Outputs
- SMA PureSignal (Predistortion) Loop Input and Output
- RJ45 Ethernet LAN Connector